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EXAMINER
CHAUHAN, ULKA J

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 03/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/056,656	PRIEM ET AL.	
	Examiner	Art Unit	
	Ulka J. Chauhan	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *100-112* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *104* is/are allowed.

6)☒ Claim(s) *100-103 and 105-112* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *19 December 2002* is: a)☒ approved b)☐ disapproved by the Examiner

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *37* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 42-61, 70-81, and 90-99 are cancelled; claims 100-112 are newly added and pending.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 100-102 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 100 lines 9-10 recite that "said replacement policy determination operates such that a common priority scheme is applied to a plurality of cache lines containing texels". The specification discloses a least recently loaded replacement scheme at pg. 20, but there is no disclosure of a "common priority scheme".

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. **Claims 100-102 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,987,567 to Rivard et al and U.S. Patent No. 5,696,892 to Redmann et al.**

7. As per claim 100, Rivard teaches a computer system 600 comprising a bus 620 ("a bus") coupled to a CPU 605 ("a central processing unit") and a graphics accelerator 635 ("a graphics accelerator") at Fig. 6. Rivard discloses that the graphics accelerator includes graphics pipeline stages including texture mapping stage 645 and a texel cache system 650 ("a texture cache system") comprising cache tags 1010,1015 and cache data store 1030 ("a texture cache memory") [col. 6 lines 22-26 and Figs. 6, 10]. Rivard further discloses that the cache tag blocks 1010, 1015 determine whether requested texel values are stored in the cache data store 1030 and include LRU engines to compute the least recently used cache address [col. 6 lines 39-40 and col. 7 lines 49-55]. Rivard discloses a most-recent texel cache data storage for a number of the most-recently-retrieved texels and a line-to-line texel cache data storage for a previously-retrieved adjacent line of texels where the most-recently-retrieved texels and the adjacent line of texels reflect the best estimation of information which will be needed and redundant for the interpolative sampling computations ("a common priority scheme is applied to a plurality of cache lines") [col. 3 lines 11-18].

8. As per claim 100, Rivard does not expressly teach a DMA engine that retrieves texel data from memory. Redmann teaches a computer graphics system including a texture memory in

which textures are loaded under the control of a DMA controller [col. 7 lines 37-53 and Fig. 1]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Rivard and Redmann such that the graphics accelerator of Rivard's invention is made to include a DMA controller as taught by Redmann whereby the texture data is retrieved from memory using DMA for faster data retrieval.

9. As per claim 101, Rivard discloses that the texel cache system 650 comprises cache tags 1010,1015 that determine whether requested texel values are stored in the cache data store 1030 and include LRU engines to compute the least recently used cache address [col. 6 lines 39-40, col. 7 lines 49-55, and Figs. 10 & 12].

10. As per claim 102, Rivard does not expressly teach 64 cache lines each storing 64 texels. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have implemented the cache data store 1030 in Rivard's invention with the capability of storing a particular amount of data such as 64 cache lines each storing 64 texels to ensure optimum cache hits.

11. **Claim 103 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,987,567 to Rivard et al and U.S. Patent No. 5,696,892 to Redmann et al and U.S. Patent No. 5,301,287 to Herrell et al.**

12. As per claim 103, Rivard does not expressly teach a DMA engine implementing a virtual-physical address translation. Herrell teaches a DMA processor 222 that comprise a small TLB having four fully associative entries, and performs an address translation for virtual pointers by doing a TLB lookup to find the physical address of the data [col. 8 lines 44-58, col. 11 lines 28-33 and lines 51-55]. It would have been obvious to one of ordinary skill in the art at the time the

invention was made to have combined the teachings of Rivard, Redmann, and Herrell such that the graphics accelerator of Rivard's invention is made to include the DMA processor as taught by Redmann that performs virtual to physical address translations using a TLB as taught by Herrell, whereby texture data is retrieved from memory using DMA for faster data retrieval using virtual addressing.

13. **Claims 111 and 112 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,790,130 to Gannett and U.S. Patent No. 5,831,640 to Wang et al.**

14. As per claim 111, Gannett discloses that in one embodiment of the invention, a texture mapping computer graphics system is provided including a host computer having a system memory that stores texture data ("storing a plurality of texture maps in a main memory"), and a graphics hardware device having a local memory ("local memory of a graphics accelerator") that stores at least a portion of the texture data stored in the system memory, and that renders texture mapped images [col. 5 lines 55-65]. Gannett discloses that a software daemon running on a processor of the host computer, manages transfers of texture data from the system memory to the local memory when needed by the hardware device to render an image ("transferring a subset of said plurality of texture maps from the main memory to a local memory" and "accessing texels from ...the local memory") [col. 5 lines 62-65 and col. 9 lines 7-20]. Gannett does not expressly teach both a local memory and a cache in the graphics accelerator. Wang discloses a graphics hardware system 108 includes a texture engine 10 having a TDA circuit 200, that processes texture map data request addresses so that useful texture map data is supplied from a cache memory 251 ("caching the texels") to the filter 260 simultaneously during a fetch interval wherein other texture data is being fetched from a local frame buffer 110 ("accessing texels ...in

the local memory") [col. 6 lines 53-61]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Gannett and Wang such that the computer graphics system of Gannett's invention includes both a local memory and a cache memory in the graphics hardware device so that an additional level of caching is implemented using the local memory as an intermediate level between the texture cache and the system memory for the purpose of improving texture data accesses.

15. As per claim 12, Gannett discloses that the cache memory is divided into two banks, with blocks 0-31 lying in bank zero, and blocks 32-63 lying in bank one, and that the cache directory includes up to sixty-four block tag entries that correspond to the blocks in the cache [col. 32 lines 23-29]. Gannett discloses that the physical location of each block tag within the cache directory identifies the physical location of the corresponding block of texture data within the cache memory [col.32 lines 23-39].

Claim Rejections - 35 USC § 102

16. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

17. Claims 105-110 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 5,790,130 to Gannett.

18. As per claim 105, Gannett teaches a graphics system in which the texture mapping board 12 includes a cache memory 48 that stores texture MIP map data associated with primitives

being rendered ("caching a first plurality of texel values"), and that interpolates the primitive data to compute the screen display pixels that represent the primitive, and determines corresponding resultant texture data for each primitive pixel ("generating a first plurality of pixel texture values" and "generating a second plurality of pixel texture values") [col. 13 lines 44-55]. The texture mapping board including chip 46 interpolates the x,y pixel coordinates and interpolates S and T coordinates that correspond to each x,y screen display pixel that represents the primitive and for each pixel, accesses the portion of the texture MIP map that corresponds thereto from the cache memory, and computes resultant texture data for the pixel ("reusing at least one of the first plurality of cached texel values") [col. 14 lines 1-9]. Gannett discloses that the texture mapping board operates upon triangle primitives where the data representing the triangle primitives includes the coordinates S,T of the portions of the texture map that correspond to the at least one vertex ("defining a texture over a first triangle") [col. 13 lines 60-67]. Gannett further discloses that a cache miss occurs if the corresponding texels for the primitive pixel are not stored in the cache memory when accessed by the texture mapping chip 46 and the *needed portion* of the texture MIP map data is downloaded from the main memory 17 into the cache memory 48 ("caching a second plurality of texel values ... less in number than the first") [col. 14 lines 37-49].

19. As per claim 106, Gannett discloses that the texture mapping board operates upon triangle primitives where the data representing the triangle primitives includes the coordinates S,T of the portions of the texture map that correspond to the at least one vertex ("defining a texture over a second triangle") [col. 13 lines 60-67].

20. As per claim 107, Gannett discloses that the front-end board, texture mapping board, and frame buffer are each pipelined and operate on multiple primitives simultaneously at col. 12 lines 65-67. And Gannett discloses that texture data for any primitive is downloaded into the local memory 48 before it is needed by the primitive at col. 42 lines 38-51.

21. As per claim 108, Gannett discloses that for each display screen pixel that is rendered with texture data from a two-dimensional texture map, as many as four texels from one MIP map (for bilinear interpolation) may be accessed from the cache memory to determine the resultant texture data for the pixel and that the texels read from the cache are provided to the texel interpolator 76, which interpolates the multiple texels to compute resultant texel data for each pixel [col. 20 line 60–col. 21 line 1]. Gannett discloses that the cache memory 48 includes four interleaves 204A, 204B, 204C and 204D [Fig. 7] and that four controllers can simultaneously access data from the four interleaves [col. 21 lines 55-60]. And Gannett discloses that texel data downloaded to the cache is organized in the main memory so that any four adjacent texels in each MIP map are located in separate interleaves so that they can be accessed in parallel; thus, any four adjacent texels in a MIP map that may be needed to generate resultant texel data through bilinear interpolation can be read in a single read operation [col. Lines 21 line 66-col. 22 line 6].

22. Claims 109 and 110 are similar in scope to claims 105 and 106, and are rejected under the same rationale.

Allowable Subject Matter

23. Claim 104 is allowed.

24. The following is a statement of reasons for the indication of allowable subject matter: the cited prior art does not disclose or render obvious the combination of elements recited in the claim, including, a graphics accelerator having a texture cache system operating in a pre-fetch mode, pre-fetching a set of texels if it is determined that the set of texels can fit into one half of the texture cache memory as per claim 104.

Response to Arguments

25. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

26. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

27. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Ulka Chauhan** whose telephone number is **(703) 305-9651**. The

examiner can normally be reached Mon.-Fri. from 9:00 am to 4:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Matthew Bella**, can be reached at **(703) 308-6829**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

29. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 305-4700.

Ulka J. Chauhan
Primary Examiner
Art Unit 2676

ujc
March 9, 2003